Fig. 1

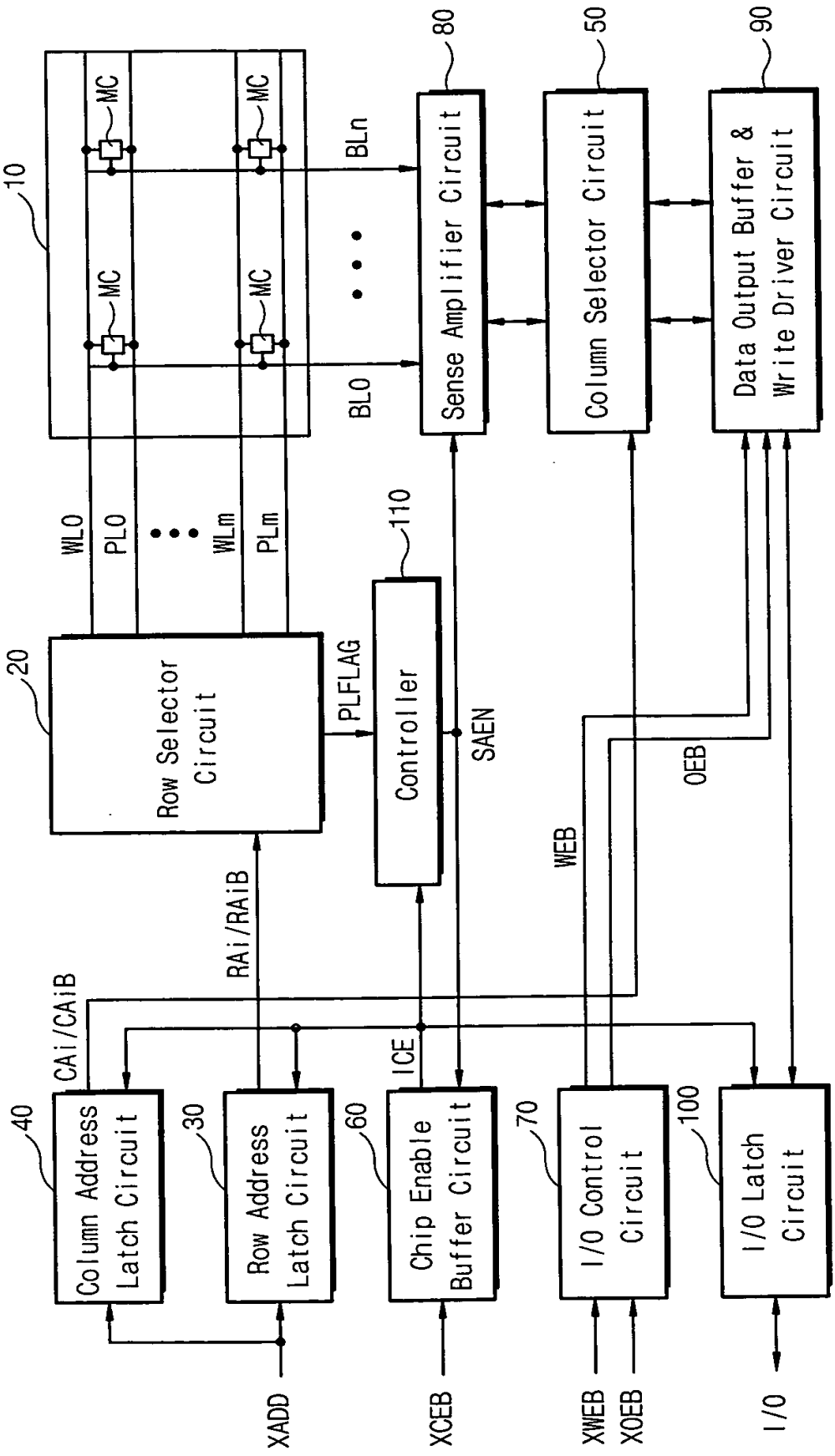

10
MC
BLn
BL0
80
Sense Amplifier Circuit
50
Column Selector Circuit
90
Data Output Buffer & Write Driver Circuit
WL0
PL0
WLm
PLm
110
Controller
20
Row Selector Circuit
PLFLAG
SAEN
OEB
WEB
RAi/RAiB
CAi/CAiB
ICE
40
Column Address Latch Circuit
30
Row Address Latch Circuit
60
Chip Enable Buffer Circuit
70
I/O Control Circuit
100
I/O Latch Circuit
XADD
XCEB
XWEB
XOEB
I/O

Fig. 2

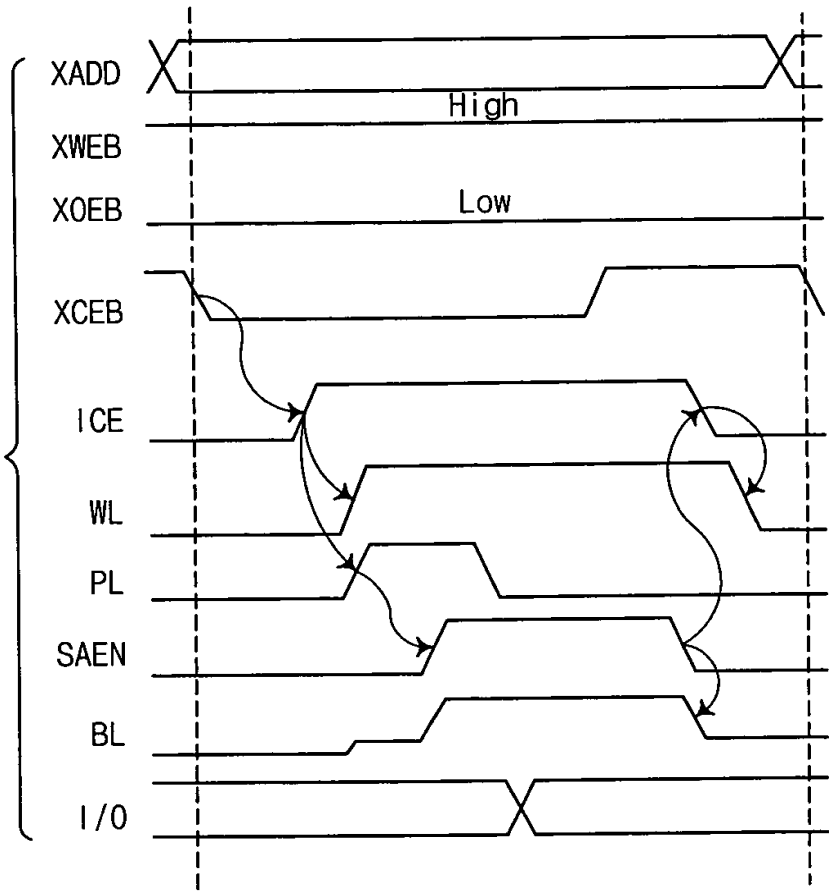


Fig. 3

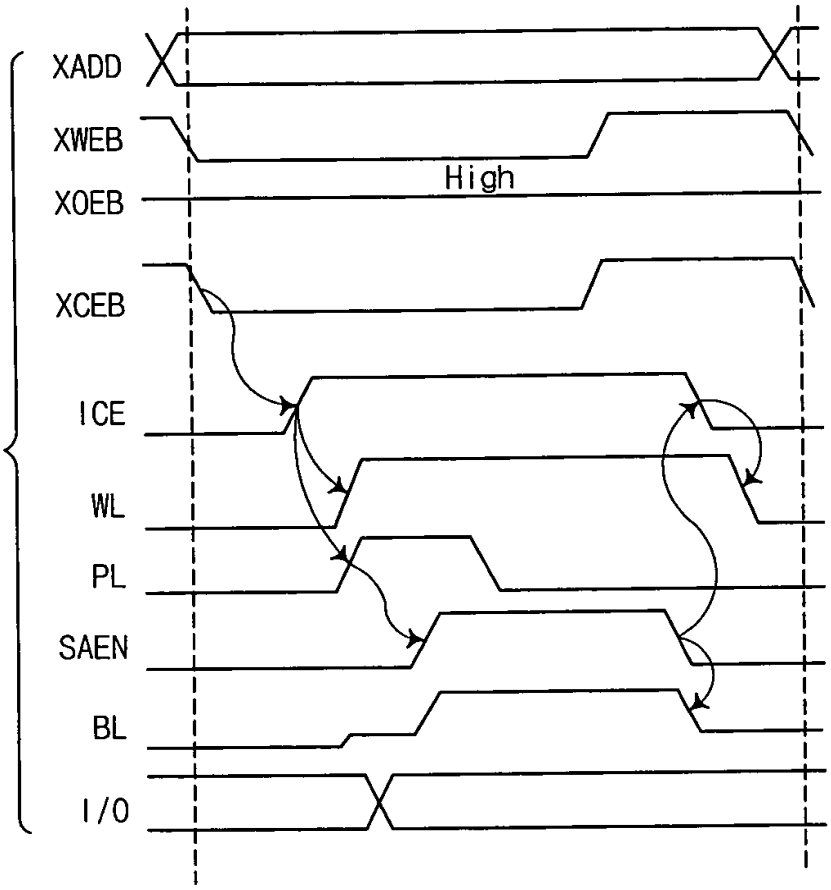


Fig. 4

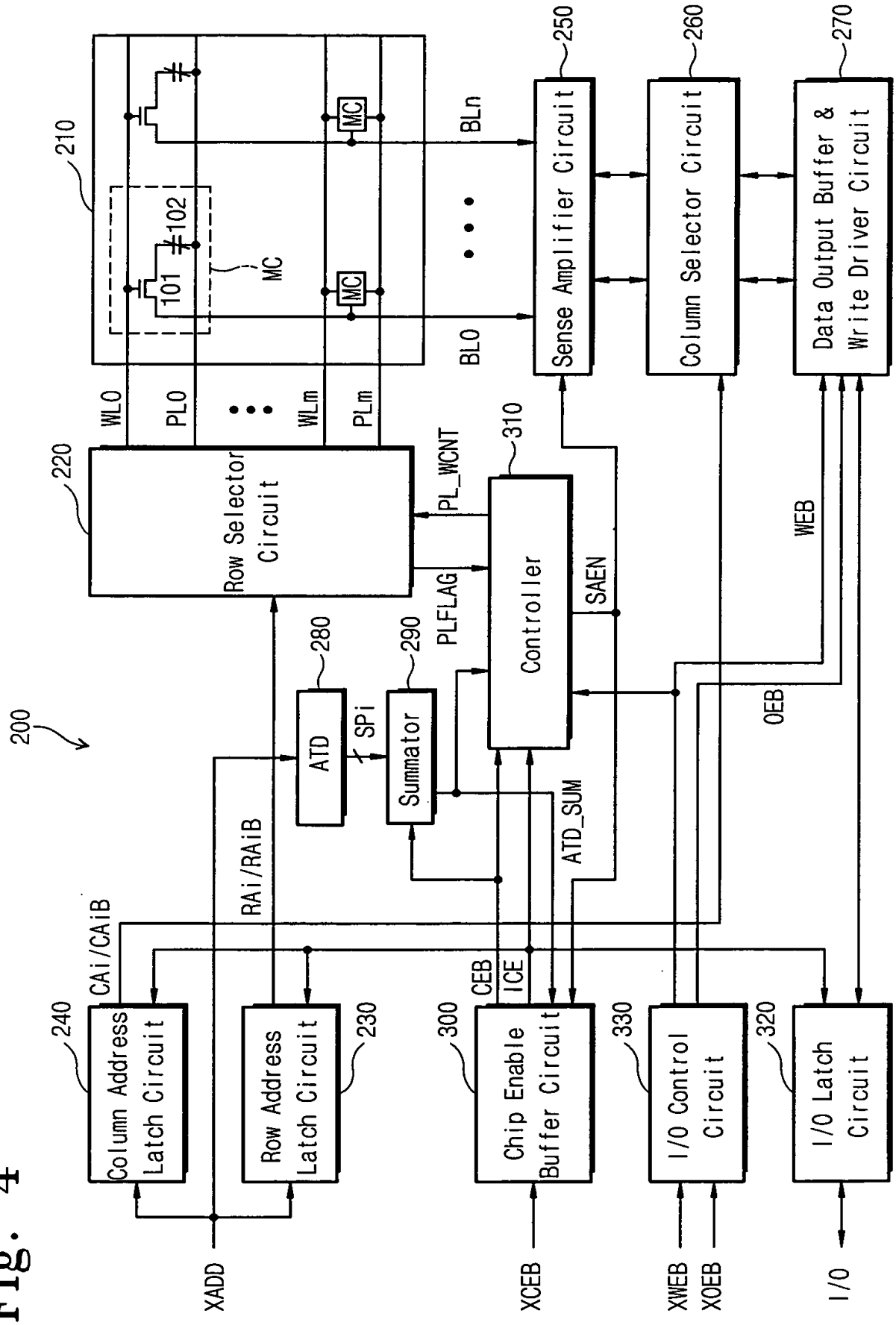

200
210
220
240
230
300
330
320
250
260
270
280
290
310
MC
101
102
WL0
PL0
WLm
PLm
BLn
BL0
Row Selector Circuit
Column Address Latch Circuit
Row Address Latch Circuit
Chip Enable Buffer Circuit
I/O Control Circuit
I/O Latch Circuit
Sense Amplifier Circuit
Column Selector Circuit
Data Output Buffer & Write Driver Circuit
ATD
SPi
Summator
Controller
PL_WCNT
PLFLAG
SAEN
ATD_SUM
WEB
OEB
CEB
ICE
CAi/CAiB
RAi/RAiB
XADD
XCEB
XWEB
XOEB
I/O

Fig. 5

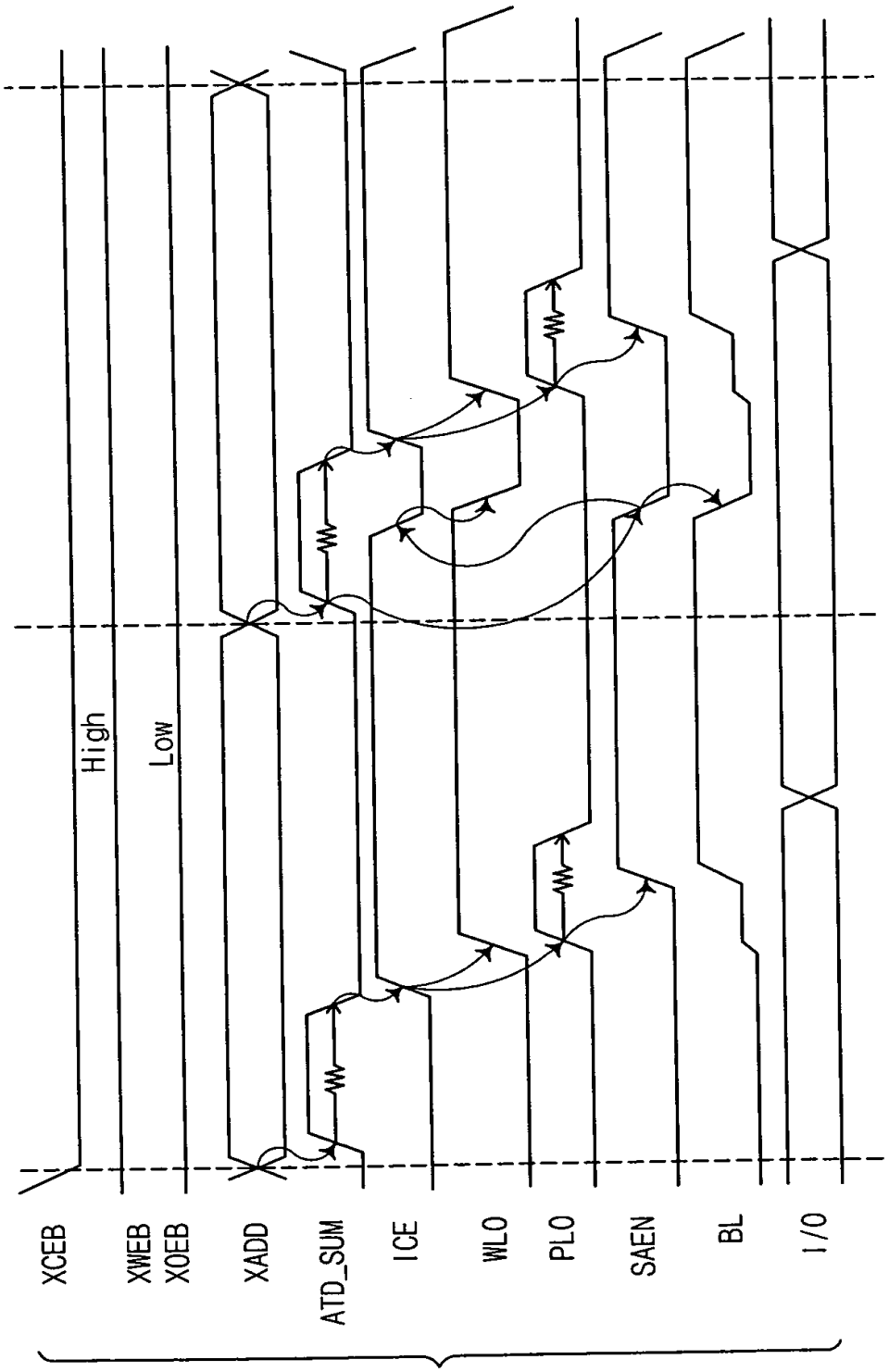
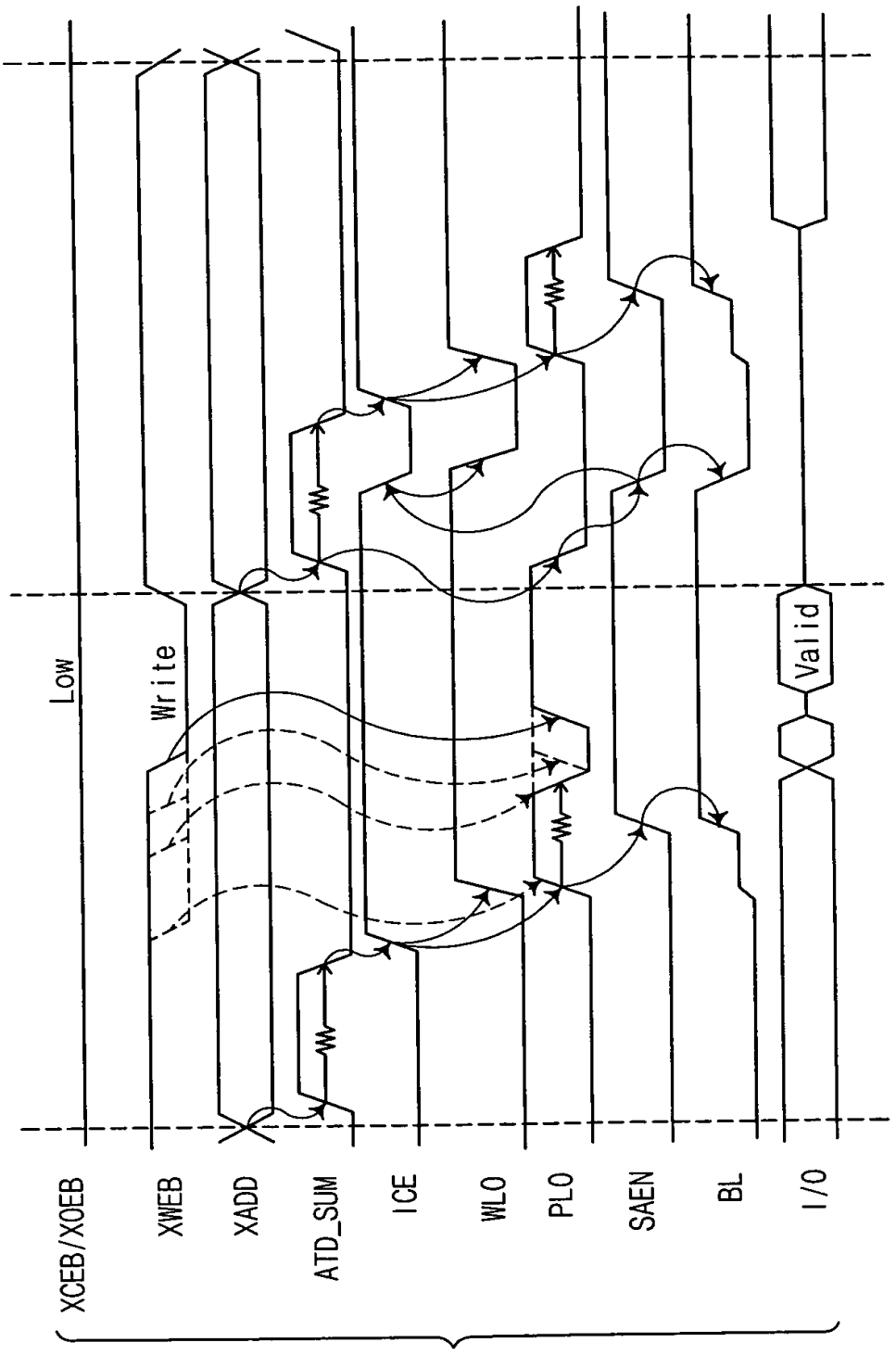


Fig. 6


Low
Write
Valid
XCEB/XOEB
XWEB
XADD
ATD_SUM
ICE
WLO
PLO
SAEN
BL
I/O